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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,759	04/14/2004	Stephen G. Holmes	NVID-P000905	7064

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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,759	HOLMES, STEPHEN G.	
	Examiner	Art Unit	
	Walter F. Briney III	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/24/2005 and 4/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claim 8 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in a telephonic interview with Eric Gash, Reg. No. 46,274, on 11 July 2007. For the record, claims 1-6 and 9-25 are considered generic, but claims 7 and 8 were drawn to mutually exclusive species.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaalaas et al. (US Patent 6,226,758 B1) in view of Sundqvist et al. (US Patent Application Publication 2004/0071132 A1).**

Claim 10 is limited to "a method for synchronizing audio processing modules." Relying on the combination of Gaalaas and Sundqvist alone, this claim is rendered obvious. To wit, Sundqvist teaches detecting the bit rate of the input and output processing modules in paragraphs [0041] and [0042]. This corresponds to "registering a plurality of audio processing modules." Step 202, where it is determined if the clocks match, corresponds to "determining if an associated set of audio processing modules

utilize a common clock source." When taken in combination with the base disclosure of Gaalaas, the teachings of Sundqvist require that the first processing module switch and second processing module switch are configured to bypass the sample rate converter when their clocks match. This results in data being transferred directly between the two processing modules by way of "a first buffer" 203. Therefore, Gaalaas in view of Sundqvist makes obvious all limitations of the claim.

2. **Claims 1-7, 9 and 11-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaalaas in view of Sundqvist and further in view of Linz (US Patent 6,005,901).**

Claim 1 is limited to "an electronic audio system." In rejecting this claim, reference is made to US Patent 6,226,758 B1 (herein Gaalaas). Gaalaas teaches a sample rate conversion of non-audio AES data channels; however, Gaalaas also provides for sample rate conversion of audio data channels as disclosed in column 5, lines 47-67, and column 6, lines 1-6. As seen in figure 2, audio data from the serial audio input 201 is passed either to a sample rate converter 202 to a serial audio output 203 or directly to the output 203. The available sources and sinks of audio data include ADC 108, DAC 106 and DSP 101, which figure 1 illustrates in communication with the digital audio I/O circuit 102 detailed in figure 2. Again, see column 5, lines 47-67, and column 6, lines 1-6. These represent "a first audio processing module and a second audio processing module." The claimed "sample rate converter" corresponds to sample rate converter 202 within circuit 102; however, no "clock manager communicatively coupled to said first and second audio processing modules" exists. Instead the user alone configures the sample rate converter. See column 6, lines 3-6.

Moreover, there is no disclosure of "a buffer." These two deficiencies are overcome by obvious modifications to Gaalaas.

First, it would have been obvious to automatically switch between datapaths, one using a sample rate converter and another without, in accordance with the teachings of Sundqvist. In operation, the method of Sundqvist detects whether the sample rates of an input and output are matched to properly enable or disable the sample rate converter. See figures 2 and 4 as well as paragraph [0048]. When conversion is not needed and the converter is taken out of circuit, it follows that less power is consumed and less delay introduced in processing audio signals. The control module 401 corresponds to the claimed "clock manager" since it determines "a first clock source" and "a second clock source." See paragraphs [0041] and [0042]. When imported into Gaalaas, the control module 401 must control both switches upstream and downstream from sample rate converter 202, so that it is "communicatively coupled to said first and second audio processing modules." In this way, the clock manager taught by Sundqvist configures "said first and second audio processing modules...as a function of said first clock source and said second clock source." Still, the act of "configuring a sample rate converter" has not been shown, but becomes evident upon considering how the sample rate converter operates.

Before discussing the sample rate converter's operation, one of ordinary skill in the art must choose a sample rate converter. Gaalaas suggests using an asynchronous converter, for example, the converter taught by Linz. See column 2, lines 1-19. The converter of Lenz includes two buffers, 28 and 12, which are synchronized using

convolver 32. As seen in figure 1, accumulator 22 uses clock information from both input and output clocks to manage synchronization between the two buffers. See column 4, lines 25-67, and column 5, lines 1-46. In this way, "configuring a sample rate converter as a function of said first clock source and said second clock source" occurs. Also, buffers 28 and 12 correspond to the claimed "buffer communicatively coupled to a first audio processing module and a second audio processing module."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Gaalaas to automatically switch between sample rate converting datapaths as taught by Sundqvist for the purpose of automating datapath management and increasing operation efficiency and to embody element 202 with the sample rate converter taught by Linz since Gaalaas is silent regarding the superiority of any particular converter, however, suggesting the efficacy of the asynchronous design used by Linz.

Claim 2 is limited to "the audio system according to claim 1," as covered by Gaalaas in view of Sundqvist and further in view of Linz. As set forth in the rejection of claim 1, the DSP 101 could be the first processing module while DAC 106 is the second processing module. In this way, the "first audio processing module comprises an accelerator module" and the "second audio processing module comprises a renderer module." Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 3 is limited to "the audio system according to claim 1," as covered by Gaalaas in view of Sundqvist and further in view of Linz. As set forth in the rejection of

claim 1, the DSP 101 could be the first processing module while DAC 106 is the second processing module. In this way, the "first audio processing module comprises a local stage" and the "second audio processing module comprises a global stage." Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 4 is limited to "the audio system according to claim 1," as covered by Gaalaas in view of Sundqvist and further in view of Linz. As set forth in the rejection of claim 1, the ADC 108 could be the first processing module while DSP 101 is the second processing module. In this way, the "first audio processing module comprises a first accelerator module" and the "second audio processing module comprises a second accelerator module." Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 5 is limited to "the audio system according to claim 1," as covered by Gaalaas in view of Sundqvist and further in view of Linz. As set forth in the rejection of claim 1, the ADC 108 could be the first processing module while DSP 101 is the second processing module. In this way, the "first audio processing module comprises a first local stage" and the "second audio processing module comprises a second local stage." Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 6 is limited to "the audio system according to claim 1," as covered by Gaalaas in view of Sundqvist and further in view of Linz. This claim requires that the first audio processing module and second audio processing module use a shared buffer

to transmit data when their clocks are common. Gaalaas and Sundqvist provides this feature where the clock manager of Sundqvist detects a common clock and bypasses the sample rate converter. This results in the upstream/first processing module switch and downstream/second processing module switch being configured in their top positions. It follows that data is routed between the first and second processing modules directly by shared buffer 203. Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 7 is limited to "the audio system according to claim 1," as covered by Gaalaas in view of Sundqvist and further in view of Linz. This claim requires that the first audio processing module output data to an input portion of said buffer and that said second audio processing module retrieve said output data from an output portion of said buffer after the sample rate converter modifies the output data by either adding or deleting samples from the input portion. When the clock manager of Sundqvist detects mismatched clocks and activates the sample rate converter, control flows to the converter taught by Linz. Therein, the convolver 32 decimates and interpolates samples placed in delay line 28—the input portion of said buffer—by input 10, which corresponds to the first audio processing module. See column 3, lines 13-25, and column 6, line 56, through column 8, line 19. In this way, convolver corresponds to the "sample rate converter," per se. This results in FIFO 12 corresponding to "said output portion of said buffer." Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 9 is limited to "the audio system according to claim 1," as covered by Gaalaas in view of Sundqvist and further in view of Linz. The first and second clock source are determined by Sundqvist using "global unique identifiers." The first is the actual monitored bit rate of the input audio stream while the second global unique identifier is read from memory. See paragraphs [0041] and [0042]. Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 11 is limited to "the method according to claim 10," as covered by Gaalaas in view of Sundqvist. The method steps recited herein are analogous to those treated in the rejection of claim 7, and are rejected for the same reasons—including the obvious incorporation of the teachings of Linz. Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 12 is limited to "the method according to claim 11," as covered by Gaalaas in view of Sundqvist and further in view of Linz. According to figure 1 of Gaalaas, the first processing module could be ADC 108, which generates an output as a function of "one or more received sounds," as evidenced by its connection to microphone 109. Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 13 is limited to "the method according to claim 11," as covered by Gaalaas in view of Sundqvist and further in view of Linz. When the second processing module is the DAC 106 disclosed by Gaalaas, it follows that the DAC renders a playback signal as a function of said first set of audio data passed directly to buffer 203 when the

processing modules utilize said common clock source, and that the DAC renders a playback signal as a function of said second set of audio data generated by the sample rate converter 202 when the modules do not utilize said common clock source. Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 14 is limited to "the method according to claim 11," as covered by Gaalaas in view of Sundqvist and further in view of Linz. When the second processing module is the DSP 101 disclosed by Gaalaas, it follows that the combination of the DSP and drive unit 105 record an input signal as a function of said first set of audio data passed directly to buffer 203 when the processing modules utilize said common clock source, and that the DSP 101 and drive unit 105 record an input signal as a function of said second set of audio data generated by the sample rate converter 202 when the modules do not utilize said common clock source. Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 15 is limited to "the method according to claim 11," as covered by Gaalaas in view of Sundqvist and further in view of Linz. When the DSP 101 is the first processing module, it "processes said first set of audio data." Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 16 is limited to "the method according to claim 11," as covered by Gaalaas in view of Sundqvist and further in view of Linz. When the DSP 101 is the second processing module, it "processes said first set of audio data, when said associated set of audio processing modules utilize said common clock source; and processes said

second set of audio data, when said associated set of audio processing modules do not utilize said common clock source." Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 17 is limited to "a method for synchronizing audio processing modules." Importing the combination of Gaalaas, Sundqvist and Linz set forth in the rejection of claim 1 results in the claimed method. When the clock manager of Sundqvist detects that the clocks are the same, it cuts the sample rate converter from the datapath so that audio data is passed form the first audio processing module, e.g. 108, directly to the second module, e.g. 106, by way of shared buffer 203 Otherwise, when the clocks are different, the audio data is processed in accordance with the teachings of Linz, which require storing audio data in an input buffer 28, receiving audio data consumed by the second processing module from output buffer 12 and synchronizing the flow rates of the buffers using the convolving filter 32 portion of decimation filter 11. Therefore, Gaalaas in view of Sundqvist and Linz makes obvious all limitations of the claim.

Claim 18 is limited to "the method according to claim 17," as covered by Gaalaas in view of Sundqvist and further in view of Linz. Sundqvist teaches "determining a clock source of each audio processing module." See paragraph [0041] and [0042].

Claim 19 is limited to "the method according to claim 18," as covered by Gaalaas in view of Sundqvist and further in view of Linz. The determination performed by Sundqvist involves "polling each audio processing module": either by monitoring the actual bit rate of incoming data or by reading a value stored in memory. In any case, an "identifier," namely a frequency value, is received for each clock source by these

methods. Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claim 20 is limited to "the method according to claim 17," as covered by Gaalaas in view of Sundqvist and further in view of Linz. The synchronizing process of claim 17 is further detailed herein. Linz teaches what is claimed; specifically, after receiving bits from the input buffer 28 and before storing them again in output buffer 12, bits are either deleted or added (decimation or interpolation) using convolving filter 32. See column 3, lines 13-25, and column 6, line 56, through column 8, line 19. Therefore, Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Claims 21-25 are limited to "a computing device." These last five claims will be treated together since claims 22-25 simply express where each element of the audio system is embodied in the computing device comprising a memory controller hub, a processor, a main memory and an input/output controller hub. Once again, the rejection of claim 1 is incorporated herein, providing the obvious combination of Gaalaas, Sundqvist and Linz. The DSP 101 is taken as one of the plurality of audio processing modules as well as the memory controller hub; the clock manager 401 of Sundqvist and sample rate converter of Linz are taken together as part of digital audio I/O circuit 102, which itself corresponds to the processor; ADC 108 and DAC 106 together form an input/output controller hub, where both the ADC and DAC can be considered a second audio processing module and are connected to the DSP/memory controller hub by way of circuit 102; and, finally, the buffers used in the sample rate converter taught by Linz correspond to the claimed buffer and is also taken to be the main memory. Therefore,

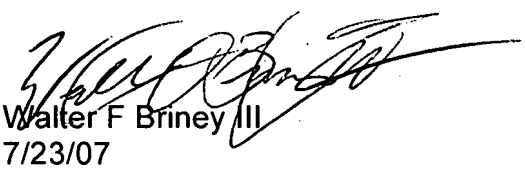
Gaalaas in view of Sundqvist and further in view of Linz makes obvious all limitations of the claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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7/23/07